VOLTAGE GENERATOR WITH REDUCED NOISE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to voltage generators, and more specifically, to a charge-pumping type voltage generator configured to reduce noise.

2. Description of the Prior Art

In conventional DRAMs, charges are pumped to generate a driving voltage for driving wordlines and bitlines without loss of threshold voltage. During DRAM operations, such as wordline-driving and bitline-precharging, a great amount of energy is consumed and then a level of the driving voltage becomes lower. In this case, the time when the level of the driving voltage becomes lower than a target level is detected in the conventional art to pump charges and maintain the level of the driving voltage.

Fig. 1 is a block diagram illustrating a conventional voltage generator. The conventional voltage generator comprises a detector 10, an oscillator 20, a control driver 30 and a pump 40. The detector 10 detects a level of a driving voltage Vpp. The oscillator 20 responds to an output signal from the detector 10. The control driver 30 responds to an output signal from the oscillator 20. The pump 40 pumps charge in response to an output signal from the control driver 30 to output the driving voltage Vpp.

Fig. 2a and 2b are circuit diagrams illustrating the conventional voltage generator of Fig. 1. The detector 10 divides the driving voltage Vpp to obtain a detection voltage Vpps. Then, the detector 10 compares the detection voltage Vpps with a reference voltage Vrc to output a low level signal when the detection voltage is larger than the reference voltage Vrc, and vice versa. The detection voltage Vpps is represented by the following equation:

$$V_{pps} = \frac{R_3 + R_4}{R_1 + R_2 + R_3 + R_4} \times Vpp$$

When the output signal from the detector 10 is at the low level, that is, the detection voltage Vpps is smaller than the reference voltage Vrc, an oscillating signal is outputted from the oscillator. The control driver 30 outputs control signals p1, p2, g1 and g2 in response to the oscillating signal from the oscillator 20. The pump 40 outputs the driving voltage Vpp, controlled by the control signals p1, p2, g1 and g2 from the control driver 30. The capacitors C1 and C2 are precharged in response to the control signals p1 and p2. The driving voltage Vpp, which is larger than an externally applied voltage Vext, is generated by transmitting the charges stored in the capacitors C1 and C2 in response to the control signal g1 and g2.

Fig. 3 is a timing diagram illustrating the operation of the conventional voltage generator. When the wordline is activated or the bitline is precharged, the level of driving voltage Vpp starts to fall. At a time of t1, the detector 10 detects that the driving voltage Vpp falls below the target level. At a time of t2,

the pump 40 starts to pump charge. The level of driving voltage Vpp rises because of the charge pumping operation of the pump 40. At a time of t3, the detector 10 detects the driving voltage Vpp at the target level, and commands the pump 40 to stop pumping charge. However, it is at a time of t4 that the actual pumping operation of the pump 40 stops due to the response time of the circuit.

As described above, in the conventional voltage generator, fluctuation ΔVpp of the driving voltage Vpp becomes large, due to the time delay between the point when the detector 10 actually detects the target level and the point when the pump 40 starts or stops operating, which results in unnecessary power consumption. Importantly, this fluctuation of the driving voltage causes noise that may destabilize the power source.

SUMMARY OF THE INVENTION

The present invention has an object to reduce fluctuation of driving voltage Vpp by pumping a predetermined amount of charge according to an operation of a DRAM when the driving voltage Vpp reaches a predetermined level before a target level.

In an embodiment of the present invention there is provided a voltage generator comprising: a detector for comparing an output voltage with a first reference voltage and a second reference voltage lower than the first reference voltage to output a first sensing signal and a second sensing signal; a controller for receiving the first sensing signal and the second sensing signal, and an action

signal to output a first control signal and a second control signal; a sub-booster for boosting a voltage in response to the first control signal; a main booster for boosting a voltage in response to the second control signal; and a voltage adder for adding output signals from the sub-booster and the main booster to provide the output voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

The disclosure will be described in terms of several embodiments to illustrate its broad teachings. Reference is also made to the attached drawings.

Fig. 1 is a block diagram illustrating a conventional voltage generator.

Fig. 2a and 2b are circuit diagrams illustrating the conventional voltage generator.

Fig. 3 is a timing diagram illustrating the conventional voltage generator.

Fig. 4 is a block diagram illustrating a voltage generator according to an embodiment of the present invention.

Fig. 5 is a timing diagram illustrating the voltage generator according to an embodiment of the present invention.

Fig. 6a is a circuit diagram illustrating a detector of Fig. 4.

Fig. 6b is a block diagram illustrating an action decoder for generating an action signal ACT of Fig. 4.

Figs. 6c and 6d are block diagrams illustrating a controller of Fig. 4.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will be described in detail with reference to the attached drawings.

Fig. 4 is a block diagram illustrating a voltage generator according to an embodiment of the present invention.

In this embodiment, the disclosed voltage generator comprises a detector 100, a controller 200, a main oscillator 300, a sub-oscillator 310, a main control driver 400, a sub-control driver 410, a main pump 500, a sub-pump 510 and a voltage adder 600. The detector 100 has more than two detection levels. The controller 200 outputs a control signal when an action signal ACT is inputted after a driving voltage Vpp passes a predetection level and before a driving voltage Vpp reaches a target level. The main oscillator 300 and the sub-oscillator 310 output oscillating signals in response to the control signal outputted from the controller 200. The main control driver 400 and the sub-control driver 410 output pump control signals in response to the oscillating signals outputted from the main oscillator 300 and the sub-oscillator 310. The main pump 500 and the sub-pump 510 pump voltages in response to the pump control signals outputted from the main control driver 400 and the sub-control driver 410. The voltage adder 600 adds the voltages outputted from the main pump 500 and the sub-pump 510, and then outputs the added voltage as a driving

voltage. The driving voltage is fed back to the detector 100.

The level of driving voltage Vpp falls because of action on the memory device or charge leakage consumes charge. The point and amount of charge consumption due to a specific action can be predicted by stimulation.

The following is described using an action for activating a wordline or precharging a bitline as an example. For the purposes of this example it is assumed that the charge consumed during a wordline activation is Q1, which is obtained through stimulation, and that the reservoir capacitance is C1. When the wordline is activated, the range of fluctuation of driving voltage Vpp becomes Q1/C1. Additionally, if the charge consumption is Q2, the fluctuation of driving voltage Vpp becomes Q2/C1. Accordingly, the fluctuation of driving voltage Vpp can be reduced by pre-pumping and providing the predetermined amount of charge.

In order to prevent the level of the driving voltage Vpp from rising too high above the target level, a predetermined level that is higher than the target level is set as a predetection level and the charges are pre-pumped only when the level of the driving voltage Vpp becomes lower than the predetection level. If an action command is inputted at a point when the driving voltage Vpp is lower than the predetection level but higher than the target level, the disclosed voltage generator pre-pumps charges necessary for an action according to a given action command. As a result, the fluctuation of the driving voltage Vpp can be reduced in the disclosed voltage generator.

When the amount of charge actually consumed is larger than the predicted amount, the level of the driving voltage Vpp becomes lower than the target level. In that case, the disclosed voltage generator pumps charges in the same way as a conventional voltage generator does. When the amount of charge actually consumed is smaller than the predicted amount, the driving voltage Vpp is maintained over the target level and the DRAM performs a normal operation. In addition, since the pumping starts only when the level of the driving voltage Vpp becomes lower than the predetection level, the excessive rise of the driving voltage Vpp due to charge pumping can be prevented by properly regulating the predetection level.

Although a preferred embodiment of the present invention uses only two detection levels, one as a predetection level and the other as a target level, the number of detection levels is increased beyond two according to other preferred embodiments.

Fig. 5 is a timing diagram illustrating the voltage generator according to the present invention.

The detector 100 activates a predetection level signal del_en and a target level signal det2_en when detecting a predetection level det1 and a target level det2 (t1, t2). If the predetection level signal det1_en is activated, and an action command ACT is inputted before activation of the target level signal det2_en (t_det), the controller 200 activates a sub-pump control signal sub_pump_en. When the sub-pump control signal sub_pump_en is activated, the sub-oscillator

310, the sub-control driver 410 and the sub-pump 510 sequentially start to operate. If the target level signal det2_en is activated, the main pump 500 starts to operate after a predetermined response time. The amount of time during which the sub-pump 510 performs a pumping operation is determined by the action command ACT. Here, the period of time when the sub-pump 510 performs a pumping operation can overlap with that of the main pump 500. The sub-pumping can be stopped during the main pumping operation according to a preferred embodiment. At a time of t3, the detector 100 detects that the driving voltage Vpp is recovered to the target level. At a time of t4, the main pump 500 stops pumping charges after a predetermined response time.

Fig. 6a is a circuit diagram illustrating the detector 100 of Fig. 4. The detector 100 comprises a detection unit 120, a first comparator 110 and a second comparator 130. The detection unit 120 divides the driving voltage V_{pp} to make two detection voltages V_{pps1} and V_{pps2}. The first comparator 110 compares the detection voltage V_{pps1} with a voltage V_{rc1} corresponding to the predetection level. The second comparator 130 compares the detection voltage V_{pps2} with a voltage V_{rc2} corresponding to the target level. The detection levels V_{pps1} and V_{pps2} are represented by the following equations:

$$V_{pps1} = \frac{R_2 + R_3 + R_4}{R_1 + R_2 + R_3 + R_4} \times V_{pp}$$

$$V_{pps2} = \frac{R_3 + R_4}{R_1 + R_2 + R_3 + R_4} \times V_{pp}$$

The comparator 110 outputs a high level signal when the detection

voltage V_{pps1} becomes smaller than the voltage V_{rc1}. The second comparator 130 outputs a high level signal when the detection voltage V_{pps2} becomes smaller than the voltage V_{rc2}.

Fig. 6b is a block diagram illustrating an action decoder for generating the action signal ACT of Fig. 4.

The action decoder comprises a command decoder 50, a bank controller 60 and an address buffer and address decoder 70. The command decoder 50 receives and decodes a chip selection signal /CS, a row address strobe signal /RAS, a column address strobe signal /CAS and a write enable signal /WE to output a corresponding command signal CMD. The command signal includes active, read, write, precharge and refresh signals. The address buffer and decoder 70 receives and decodes an address. The command signal CMD and the output signal of the address buffer and decoder 70 are inputted into the bank controller 60. The bank controller 60 outputs an action signal ACT. The action signal Act includes each bank active, each bank precharge, each bank read and each bank write.

Figs. 6c and 6d are block diagrams illustrating the controller 200 of Fig. 4.

Fig. 6c shows a circuit for activating a pump selection signal pmp_sel when the action command is inputted after activation of the predetection level signal det1_en and before activation of the target level signal det2_en.

A NAND gate NAND1 performs the NAND operation on the predectection level signal det1_en and a signal obtained by inverting the target level signal det2_en. A NAND gate NAND2 performs the NAND operation on the action signal ACT and a signal obtained by inverting an output signal of the NAND gate NAND1. An output signal from the NAND gate NAND2 is activated if the action signal ACT is inputted when the predetection level signal det1_en is at a "high" level and the target level signal det2_en is at a "low" level. A latch latches the output signal from the NAND gate NAND2, and then outputs the latched signal as the pump selection signal pmp_sel.

Fig. 6d shows a circuit for outputting oscillator control signals sub_osc_en and osc_en in response to the action command ACT and the pump selection signal pmp_sel.

In the preferred embodiment illustrated in Fig. 6d, since the oscillator control signals sub_osc_en and osc_en have opposite logic levels with respect to each other, the main oscillator 300 does not operate when the sub-oscillator 310 operates. However, the main oscillator 300 and the sub-oscillator 310 can operate simultaneously in other embodiments of the present invention.

A plurality of pulses having different activation times are inputted into a multiplexer 214. Each block (block 1, block 2, ..., block n) for generating one of the plurality of pulses includes a delay circuit 211, such as an inverter chain. The delay time of the delay circuit 211 is configured to be different according to the action signal ACT. Since the multiplexer 214 selects and outputs one of the

output signals from the blocks (block 1, block 2, ..., block n) according to the action signal ACT, the time when the oscillator control signal sub_osc_en is maintained at an active state is differentiated according to the action signal ACT.

Since the sub-oscillator 310 outputs the oscillating signal only when the oscillator control signal sub_osc_en is in the active state, the amount of pumped charge can be regulated according to the action signal ACT.

Accordingly, in the disclosed voltage generator, the level of the driving voltage Vpp can be prevented from excessively fluctuating by operating the sub-pump before operating the main pump. As a result, noise which may result from excessive fluctuation of the driving voltage can be reduced. Additionally, electric power necessary for maintaining the driving voltage Vpp above the target level can be reduced because the amount of charge to be pumped decreases as the variation of the driving voltage decreases.

While the invention is susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and described in detail herein. However, it should be understood that the invention is not limited to the particular forms disclosed. Rather, the invention covers all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined in the appended claims.